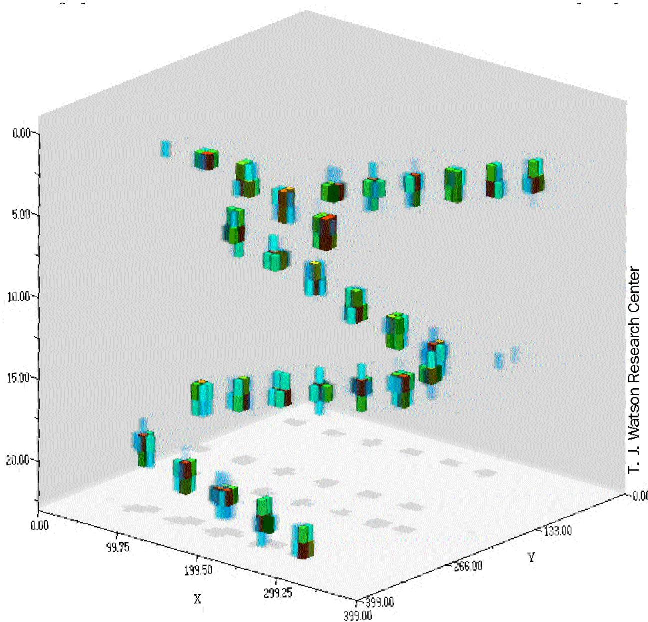
Failure Analysis in a Nanometer World

Propelled by the continuing drive for smaller features and the growing complexity of integrated circuits (ICs), failure analysis has assumed an increasingly important role in the semiconductor industry as advances in IC technology constantly outstrip the capabilities of existing detection methods. To meet the economic and performance challenges that lie ahead, researchers are devising new physical measurement methods to identify and localize the most critical faults and



tation of experimentally observed light emission from an operating ring oscillator built from CMOS inverters.

Lawrence Wagner, who heads the failure-analysis laboratory at Texas Instruments (Dallas, TX), calls the increasing difficulty in performing such analysis one of the most critical challenges facing failure analysis—especially given the complexity, new materials, and new packaging styles of devices. Today, the number of microprocessing transistors on advanced chips is between 12 and 13 million. That number is expected to increase by a factor of four within the next decade, according to the most recent predictions by Sematech, a consortium formed by leading semiconductor companies. Minimum feature sizes will decrease to 0.07 μm by 2004, significantly challenging the spatial-resolution capabilities of most existing techniques.

At the same time, the number of wiring levels is expected to increase from four today to five or six. And because defects will most likely lie buried deep within the circuitry in all but the simplest ICs, detecting and analyzing defects will transform into the proverbial needle-in-a-haystack search. “Finding a defect on the ICs that existed when I started iness was somewhat akin to losing keys at home,” says Wagner. “For today’s devices, it’s like trying to locate your lost keys from a helicopter hovering over the city of Los Angeles. By the middle of the next decade, it’s going to be like looking for our keys in the state of California.”

In addition, the gold-wire-bonding technology used to connect ICs to the outside world has become limited in performance as microprocessors approach speeds of 300 to 450 MHz. “With 300-MHz microprocessors, we can’t get the signals out because the ctance of the wire is too high,” gner. This is causing many manu- o consider a shift to flip-chip or chip-on-chip packaging. These devices sandwich internal-circuit structures between the silicon substrate and the chip, inhibiting and even preventing standard top- or front-side analysis. The emergence of flip-chip packaging thus necessitates the development of a new range of techniques employing back-side (from the substrate side) analysis. In short, says Wagner, “The tools we’ve become accustomed to using are in some jeopardy of not being able to meet our needs in the very foreseeable future.”

Sematech has identified the development of physical logic-fault isolation techniques as the industry’s top priority. Such techniques rely on an IC’s emission of, or sensitivity to, light, heat, or electrons to pinpoint failure locations. Possible faults and failures include simple short circuits that prevent a chip from operating, small leakage paths that produce early failures, and unexpected delays in the propagation of signals across a chip, which will produce logic errors only during high-speed operation.

Light-emission methods

Many IC defects produce detectable light emissions. The current technique for detecting light-emitting defects is photon emission microscopy (PEM), which involves collecting and imaging the light given off from operating ICs. The precise location of the light source is pinpointed by overlaying an image of the emitted light on a reflected-light image of the chip surface. And because the emitted photons have energies in the near-infrared (NIR) spectrum (770–1,500 nm) as well as the visible range (390–770 nm), they can also be observed from the back side of the chip.

Daniel Barton, a researcher at Sandia National Laboratories (Albuquerque, NM), has demonstrated the failure-analysis capabilities of a more advanced detector sensitive to longer infrared wavelengths, which promises to increase sensitivity for back-side PEM analysis. Inspired by a colleague at Intel, who proposed using night-vision technology to search for defects and developed a less powerful version of the device, Barton’s technique uses NIR cameras to study emission characteristics of common IC defects. The cameras evolved from a liquid-nitrogen-cooled imaging array, originally developed for infrared astronomy and installed on the Hubble Space Telescope in February 1997. They have high quantum efficiency at wavelengths of 800 to 2,500 nm, and low read noise. The cameras are the first to achieve the same level of performance in the NIR as the silicon charge-coupled-device (CCD) cameras used commercially.

To confirm the effectiveness of his approach, Barton conducted a comparison study using a nonintensified, liquid-nitrogen-cooled CCD camera. Three different defect samples were used: gate-oxide shorts, namely failures from a production lot with a high density of gate-oxide defects; a back-

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side sample, or failure from a 1.25-μm process with a known contact defect; and transistor saturation, using test transistors from a 0.05-μm CMOS process. His results clearly demonstrated that the NIR camera imaged all these defect classes with much shorter integration times than the cooled CCD, suggesting that photon emission above 1,000 nm is significantly stronger than at shorter wavelengths. The use of an NIR astronomy camera is also better for collecting light emissions through the back side of the chip because the silicon is virtually transparent at wavelengths longer that 1.1 μm.

Picosecond imaging

James Tsang and Jeffrey Kash of IBM's T. J. Watson Research Center (Yorktown Heights, NY) have developed another promising optical technique, designed primarily to detect timing-related defects. They discovered that a very weak picosecond pulse of light is emitted by each field-effect transistor in a CMOS circuit whenever the circuit changes logic state. This pulsed emission can be simultaneously imaged and a precise time established with a technique Tsang and Kash subsequently dubbed picosecond imaging circuit analysis (PICA). When combined with a suitable imaging detector, PICA allows time-resolved measurements of thousands of devices simultaneously—one of its biggest advantages in an industry where a single chip contains literally millions of transistors.

"It's like looking at New York City at night with a big video camera," says David Vallett, an advisory engineer at IBM's Microelectronics Division (Essex Junction, VT). "Other techniques that we know about only look at one 'light,' or transistor, at a time." The technique is also completely passive, in that it collects light with no need for active laser or electron beams, which relaxes the optics requirements by a factor of 2.

The computer videos made from these measurements, combined with other more quantitative evaluations of the light emission, permit the complete operation of an IC to be measured noninvasively with picosecond resolution. And unlike other analysis techniques, PICA's signal strength gets larger as IC technology gets smaller. Vallett attributes this effect to the fact that channel lengths are shrinking faster than supply voltages, which results in an increased electric field, and, therefore, an improved signal-to-noise ratio and better overall sensitivity.

Far from competing with each other, NIR arrays and PICA are best viewed as complementary, with each offering a unique capability. Both techniques image light emissions from a chip, but PICA enables analysts to study the emissions in 30-ps slices of time to isolate when a failure occurred. Although NIR arrays don't have that capability, they do enable analysts to study longer wavelengths

of light, and the signal produced is much stronger. Vallett likens NIR arrays to a 35-mm camera, in which one gathers light for as long as the shutter is open, and PICA to a video camera, which enables one to play back the switching events and isolate them into frames.

Thermal imaging

The complex wiring of today's chips makes them more sensitive to defects—such as ohmic leakage and shorts between metal conductors—that do not emit visible light and may not cause transistors to do so. Common thermal imaging techniques, such as liquid-crystal analysis and infrared thermography, are useful in detecting and analyzing them. Both, however, suffer from poor spatial resolution, especially when used for back-side analysis. A promising new thermal technique is fluorescent microthermographic imaging (FMI), developed by researchers at AT&T Bell Laboratories (Murray Hill, NJ). FMI has excellent spatial and temperature capability, with the added ability to acquire an absolute temperature map of an operating device. However, as long as the fluorescent material is located away from the heat source, as in the case of back-side analysis, spatial resolution will remain problematic.

More subtle failure mechanisms are due to nonvisual defects, and although their electrical effects can be measured, existing surface techniques such as optical microscopy and scanning electron microscopy (SEM) do not reveal these physical anomalies buried deep inside. The IC industry is heavily dependent on field-emission SEM for a wide range of defect-related applications, including critical dimension measurements, energy-dispersive X-ray analysis, and diagnostic electron-beam probing. Yet the techniques remain marginal in meeting the spatial-resolution requirements for failure analysis of 0.25-μm technology, and will most certainly be inadequate for the 0.07-μm technology looming on the horizon.

Furthermore, because their images arise from secondary electrons, SEMs cannot penetrate insulating layers to effectively probe an IC's deep structure. Higher-resolution methods such as transmission-electron and scanning-probe microscopes are robust and capable of resolving subnanometer details. But sample preparation is generally too slow, and hence too costly, for their use as routine inspection techniques. Electron-beam testing—which directs a pulse of electrons into a wire to produce secondary electrons—is widely used in the industry to glean more detailed data on the electrical behavior of circuits. The technique "provides an oscilloscope-like measurement for diagnosing defects by analyzing their effect on internal node voltages," Vallett says. It is especially well-suited for characterizing and analyzing

such time-dependent events as IC clock distribution and alternating-current or delay failures. However, on a flip-chip-mounted device, the silicon back-side is opaque to electron beams, imposing some fundamental limitations on this technology.

Full root-cause failure analysis in general is becoming prohibitively slow and expensive, especially in the wake of corporate down-sizing and the demand for quicker time-to-market. This has prompted the industry to look more closely at signature-analysis techniques. "Any data that can be gathered rapidly and allows defects to be identified individually or in groups with high confidence can be used as a signature," Vallett says.

The most likely candidate is the use of I-DDQ signatures. According to Sandia's Charles Hawkins, the I-DDQ test measures the quiescent power-supply current in a CMOS circuit. It has been used extensively in IC testing and by a small number of companies in failure analysis. Hawkins reports that 1996 experiments by Sematech and Hewlett-Packard demonstrated that this sort of test is sensitive to numerous failure mechanisms, and that it uniquely detected many more defects than such common forms of testing as stuck-at-fault models, and delay and functional testing.

Instead of a single measurement, I-DDQ is recorded as the power supply voltage (VDD) is swept from zero to a maximum value. Different types of defects provide unique signatures. "It is easy to visualize the difference between a bridging short between the power rails and one between nodes in the signal paths," says Hawkins. The method is rapid and can be used on CMOS parts that are designed for static operation. It is an especially useful technique for multilevel metals in which the surface topology is not visible. However, while I-DDQ indicates what type of defect may be present, it does not pinpoint its location.

Signature analysis with I-DDQ may enable failure analysis by inference, especially when combined with periodic validation by full physical failure analysis, which could eventually be used more as a low-throughput, periodic sampling process to validate experiments. Signature analysis also helps pave the way for a universal test platform for industry-wide use. Historically, failure analysts have used a separate test platform for doing diagnostic work. That, says Wagner, is also bound to change. "As the devices become more complex, we're going to be driven to use one test platform," he says. "We simply won't be able to afford the expense—given flip-chip packaging, cycle-time requirements, and device complexities—to have our stand-alone systems."

Further Reading

David Vallett and Jerry Soden, "Finding Fault with Deep Sub-Micrometer ICs," *IEEE Spectrum*, October 1997.