

Hybrid Semiconductor–Molecular Nanoelectronics

Ultradense integrated circuits with features smaller than 10 nm would provide enormous benefits for all information technologies, including computing, networking, and signal processing. However, recent results indicate that the current very large-scale integrated circuit paradigm based on complementary metal oxide semiconductor (CMOS) technology cannot be extended into this region. The main reason is that below a 10-nm gate length, the sen-

should be below ~ 1 nm, far too small for current and even forthcoming lithographic techniques, such as those based on extreme ultraviolet radiation and electron beams.

Hybrid circuits

Many physicists and engineers believe that this impending crisis may be resolved only by a radical paradigm shift from purely CMOS technology to hybrid semiconductor–molecular circuits, which our group

photolithography and the potentially low cost of nanoimprinting and chemically directed self-assembly. This combination may enable CMOL circuits of unparalleled density—up to 3×10^{12} functions/cm²—at acceptable fabrication costs.

For single-molecule components, single-electron devices are the leading candidate because, in contrast to field-effect transistors, their operation mechanism does not require high conductivity of the device-to-electrode interfaces. The CMOS layer allows CMOL circuits to circumvent one prominent drawback of single-electron transistors: their low voltage gain. The recent demonstration of single-molecule single-electron transistors by a Cornell University team headed by Paul McEuen and Daniel Ralph and a Bell Laboratories group led by Nikolai Zhitenev, offers hope that the first CMOL circuits will be demonstrated within the next 10 years. Hopefully, CMOL circuits will reach the industry in time to preempt the impending Moore's law crisis.

Before that, however, a host of physical, chemical, computer science, and electrical engineering problems must be solved. Notably, researchers need to bring chemically directed self-assembly from the present level of single-layer growth on smooth substrates to the reliable placement of three-terminal molecules on nanowire structures. (Two-terminal devices may be suitable for simple memories but not for more advanced circuits.)

Our group at the State University of New York at Stony Brook is working to develop and implement several molecules suitable for this purpose, an example of which is shown in Figure 1. This arrangement, suggested by Andreas Mayr, professor of chemistry at Stony Brook, essentially combines two well-known single-electron devices, the transistor and the trap. In it, diimide acceptor groups work as single-electron islands, which are sites where an additional electron can be localized. The islands are con-

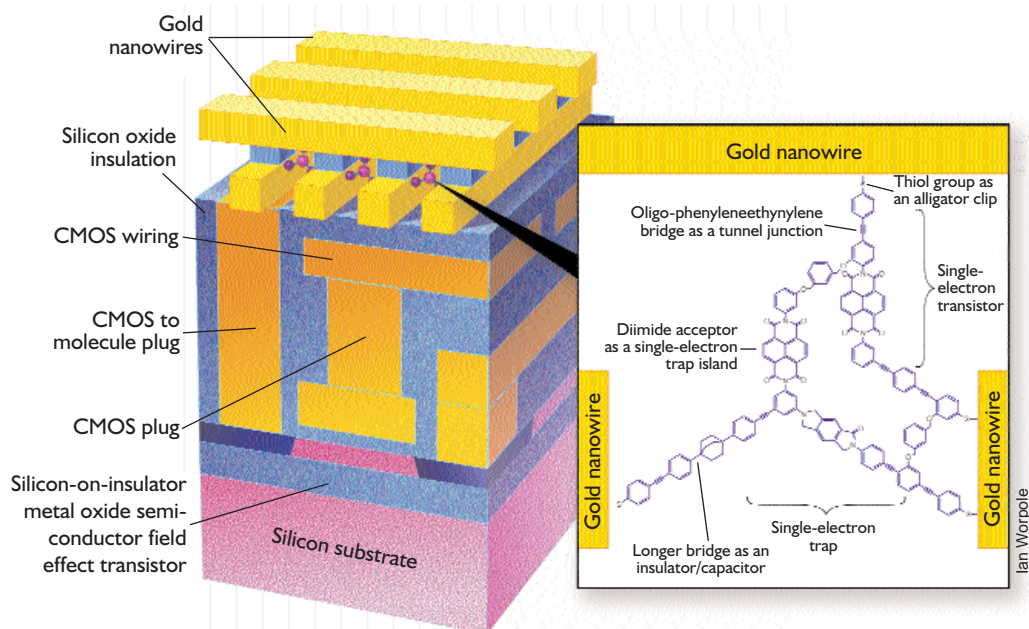


Figure 1. This hybrid complementary metal oxide semiconductor/molecular circuit contains a molecule that may function as a latching switch (including a single-bit memory cell) controlled by two input signals.

sitivity of silicon field-effect transistor parameters—most importantly, the gate-voltage threshold—to the inevitable random variations of device size grows exponentially. This sensitivity may send fabricating costs skyrocketing and lead to the end of Moore's law some time during the next decade.

The main alternative nanodevice concept—single electronics, based on controlling the motion of single electrons in solid-state structures—offers some potential advantages over CMOS technology, such as a broader choice of materials. However, the critical dimensions of single-electron transistors for room-temperature operation

has dubbed CMOL, a combination of CMOS and MOLEcular. Such a circuit (Figure 1) would combine

- a level of advanced CMOS devices fabricated by lithographic patterning,
- a few layers of parallel nanowire arrays formed, for example, by nanoimprinting,
- a level of molecular devices that self-assemble on nanowires from solution.

The CMOL concept combines the advantages of nanoscale components, such as the reliability of CMOS circuits and the minuscule footprints of molecular devices, and the advantages of patterning techniques, which include the flexibility of traditional

nected either by oligo-phenyleneethynylene bridges playing the role of tunnel junctions or by longer chains that do not conduct electrons but stabilize the geometric arrangement. All the bridges and chains are terminated by thiol groups, which serve as alligator clips and should allow molecular self-assembly on gold nanowires.

This molecule should work in the following way: when the sum of voltages applied to the top and left nanowires exceeds a certain threshold, an additional electron is injected from the right wire into the trap island. The electron's electrostatic field opens the single-electron transistor connecting the top and right wires. This connection would survive a temporary reduction of the applied voltage because it takes time for the trapped electron to escape. As a result, the device should function as a two-input latching switch, essentially a single-bit memory cell controlled by two input signals.

Neuromorphic networks

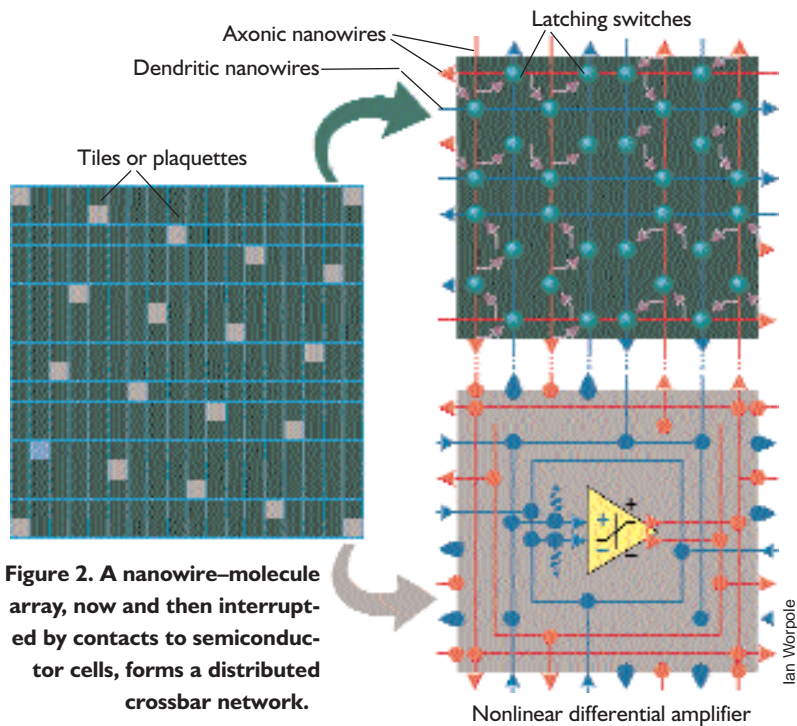
Our studies show that this device, working together with CMOS layer transistors, may enable the creation of a broad variety of highly functional integrated circuits. A family of distributed crossbar neuromorphic networks, which we have termed CrossNets, seems especially promising. Every CrossNet (Figure 2) is essentially a large field of similar tiles (or “plaquettes,” shown in green), which is now and then interrupted by contacts to “gray cells” located in the underlying CMOS layer. In this biologically inspired architecture, the latching switches (shown as green circles with arrows) serve as adaptive “synapses” that connect “axonic” nanowires (shown in red) and perpendicular “dendritic” nanowires shown in blue. The gray cells, which are essentially nonlinear differential amplifiers, serve as “somas,” or neural cell bodies.

The motivation for using neuromorphic networks comes from the well-known comparison of the performance of present-day digital computers with biological neural systems for one of the simplest tasks:

image recognition (or, more precisely, image classification). A mammal's brain recognizes a complex visual image, with high fidelity, in approximately 100 ms. Because the elementary process of neural cell-to-cell communication in the brain takes 10 to 30 ms, this means that the task takes just a few elementary operations. In contrast, the fastest modern microprocessor performing digital number crunching at a clock frequency of a few gigahertz and running the best commercially available software would require minutes (about 10^{11} clock periods) for an inferior classification of a similar image. The contrast is striking indeed.

To ensure high performance, neural networks should have very high connectivity, which is the number of other neural cells connected to any given neuron. In the cere-

bral cortex, the average connectivity is close to 10,000. The greatest advantage of CrossNet architectures is that such connectivity is automatically insured by the proper concentration of gray cells, despite the quasi-two-dimensional character of CMOS circuits. In addition, CrossNets promise an unprecedented trade-off between speed and power consumption. According to our estimates, a CrossNet circuit with a large but acceptable power of 10 W/cm² may provide an intercell communication latency of about 200 ns. Apparently slow by modern digital integrated-circuit standards, this speed is approximately 5 orders of magnitude higher than that of the network's biological prototype, the human brain. In fact, at this speed the CrossNet's computing power would be about 10^{19} bits/cm²/s—



Ian Worpole

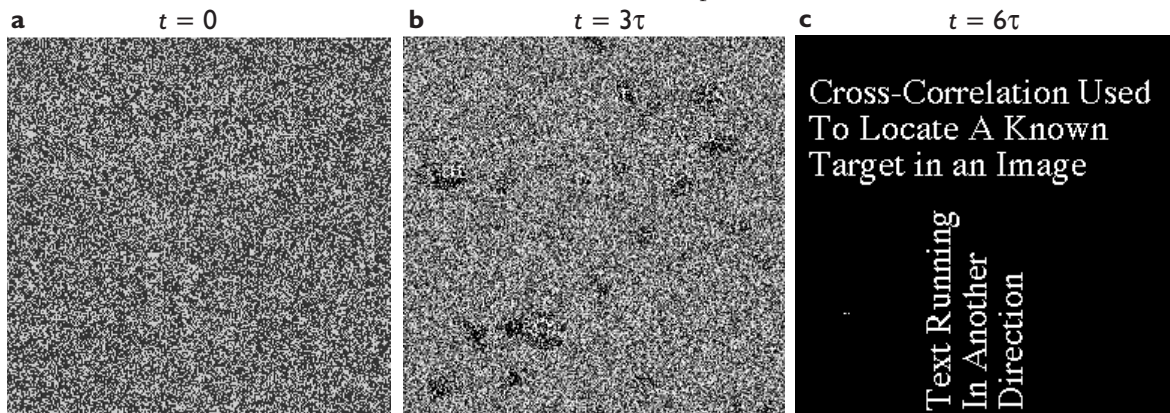


Figure 3. Image (a), obtained by flipping 40% of the pixels in image (c), was correctly restored in just six elementary time units after being shown to a distributed crossbar network trained as an associative memory.

much higher than that of any existing processor—because all 3×10^{12} molecular devices would operate in parallel.

Neuromorphic networks do not require the usual software, but they do need to be trained to perform their tasks. For Cross-Nets, the main challenge is that external access to individual synapses is impossible. Because of this, well-developed neural-network training techniques such as back-propagation cannot be used. Last December, we reported at the Sixth Molecular-Scale Electronics Conference in Key West, Florida, that despite this difficulty, we had demonstrated that at least one CrossNet species, called an InBar, may be effectively trained to operate as a Hopfield network (essentially an associative memory). Figure 3 shows the dynamics of an InBar that had been trained on a set of three different black-and-white images. After that, one of the images was spoiled by flipping 40% of the bits (left panel) and shown to the network. Very rapidly, in just 6 elementary time units, the InBar perfectly restored the initial image (right panel).

We plan to pursue our recent success in image recognition and extend our work to the more important task of image classification (the ability, for example, to recognize a human face from a totally different angle after several images of the face have been presented at training). If we succeed in that effort, even relatively small CrossNet chips may revolutionize the field of pattern analysis, including such important applications as detection of specific features, such as a tank in a satellite image.

Self-evolution

Such success would pave the way for more ambitious goals. It is plausible that a cerebral-cortex-scale CrossNet-based system—one with $\sim 10^{10}$ neurons and 10^{15} synapses that would require a $\sim 30 \times 30$ cm² silicon substrate—would be able, after initial training by a dedicated external tutor, to learn directly from its interaction with its environment. In this case, we can speak of a “self-evolving” system.

In computer science, such concepts as evolutionary computation, evolutionary


algorithms, and evolving hardware are well known. However, with CMOL circuits, we will have the first chance to merge these ideas with the enormous computing power of parallel very large-scale integrated circuits. We may be able to revisit the initial dream of neural-network science of providing the means to reproduce the natural evolution of the cerebral cortex on a much faster time scale. Such evolution could lead to self-development of such advanced features as system self-awareness (consciousness) and reasoning. If substantial success along these lines materializes, it will have a strong impact not only on information technology but also on society as a whole.

Further Reading

Likharev, K. K. Electronics below 10 nm. Submitted for publication in *Nano and Giga Challenges in Microelectronics*; Elsevier: Amsterdam, 2003. Preprint available at <http://rsfq1.physics.sunysb.edu/~likharev/nano/NanoGiga031603.pdf>.

Fendler, J. H. Chemical self-assembly for electronics applications. *Chem. Mater.* 2001, 13, 3196–3210.

Park, J.; et al. Coulomb blockade and the Kondo effect in single-atom transistors. *Nature* 2002, 417, 722–725.

Likharev, K. K.; Mayr, A.; Türel, Ö.; Muckra, I. CrossNets: High-Performance Neuromorphic Architectures for CMOL circuits. Report presented at the Sixth Molecular-Scale Electronics Conference, Key West, FL, December 2002; to be published by the New York Academy of Sciences. Preprint available at rsfq1.physics.sunysb.edu/~likharev/nano/KeyWest.pdf. 

B I O G R A P H Y

Konstantin Likharev (klikharev@notes.cc.sunysb.edu) is a Distinguished Professor of Physics at the State University of New York at Stony Brook. The Forum department is initiated by the American Physical Society's Forum on Industrial and Applied Physics (FIAP). For more information about the Forum, please visit the FIAP Web site (<http://www.aps.org/FIAP/index.html>), or contact the chair, Kenneth C. Hass (khass1@ford.com).